ABSTRACT

A system for implementing Incremental Redundancy (IR) operations in a wireless receiver includes a baseband processor, an equalizer, a system processor, a plurality of IR processing module registers, and an IR processing module. The baseband processor receives an analog signal and produces samples. The equalizer is operable to receive the samples, to equalize the samples, and to produce soft decision bits corresponding to the data block. The system processor receives the soft decision bits of the data block, configures the plurality of IR processing module registers, and initiates operations of the IR processing module. The IR processing module accesses the plurality of IR processing module registers, receives the soft decision bits of the data block, and performs IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block.